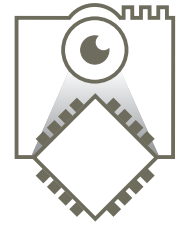


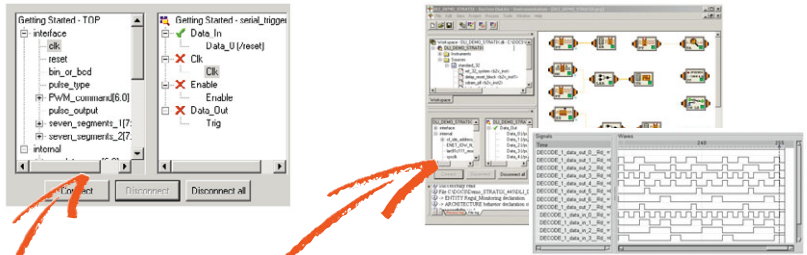
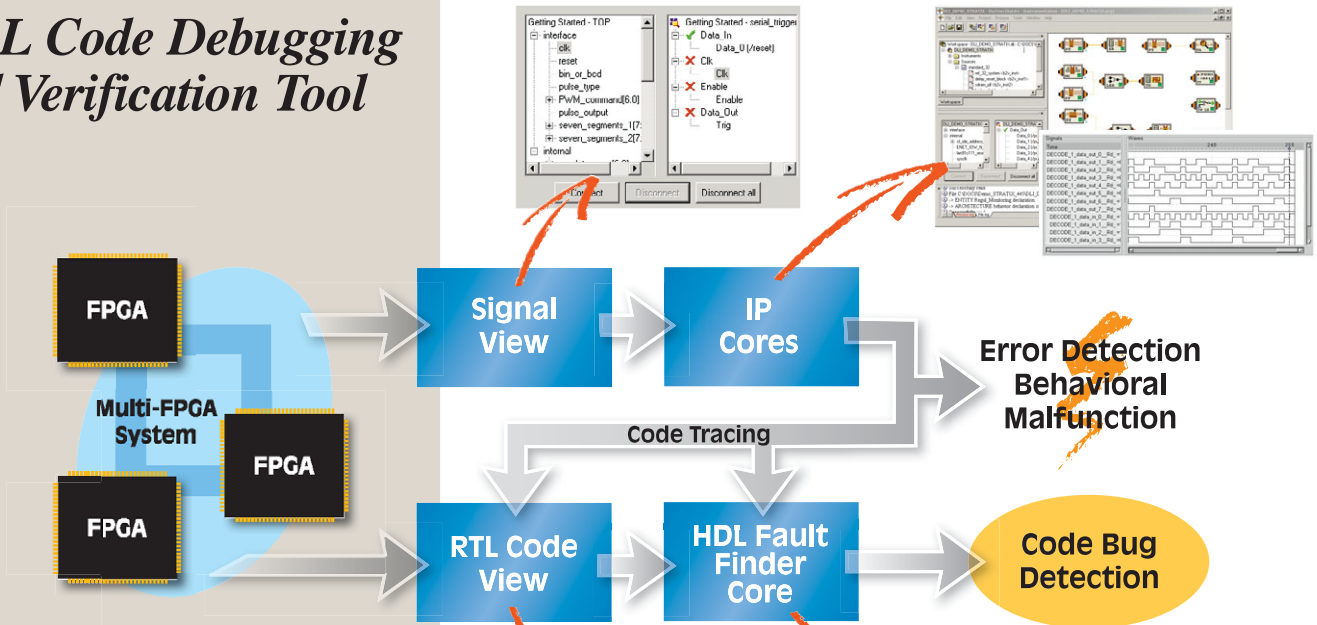


POWER EDGE EDITION

DLI™
FPGA



HDL Code Debugging and Verification Tool



OVERVIEW

DLI is an On-Chip Instrumentation tool that brings a new way to monitor and debug complex designs for any type of FPGA. Within the DLI environment, you can seamlessly choose your instrumentation inside the DLI IP Core Library and then embed it into your design. After downloading your design file and the instrumentation into your FPGA; DLI Core Control and Display Tools allows you to view all internal signals and nodes, debug, analyze logic signals and transactions, monitor busses and record logic events.

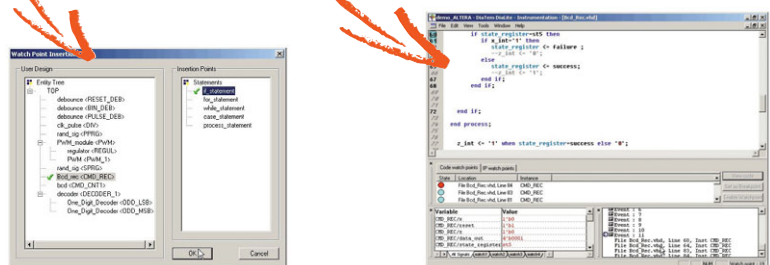
Power Edge Edition Rev 4.5 includes all features of the Leading Edge Edition plus the HDL Fault Finder module. The HDL Fault Finder allows the designer to insert Watchpoints and Breakpoints into the HDL code and run concurrently with the instrumentation. The HDL Fault Finder provides an accurate monitoring and display of logic events occurring during the debugging process. The insertion of Watchpoints in your HDL code allows you to trace all events and quickly focus on the faulty lines. In a typical situation, DiaLite allows you to use the instruments to see waveforms and detect behaviour malfunctions. Then you can use a trigger to track this bad behaviour and use it as a Hardware Breakpoint for the Fault Finder. This way, you are pointed directly towards the last lines of code that were executed before the error occurred. You are then CERTAIN that this is the code that must be corrected. **DLI THUS SAVES YOU TIME AND MAKES YOU REALLY PRODUCTIVE!**

REAL-TIME AND FASTER ON-CHIP DEBUGGING

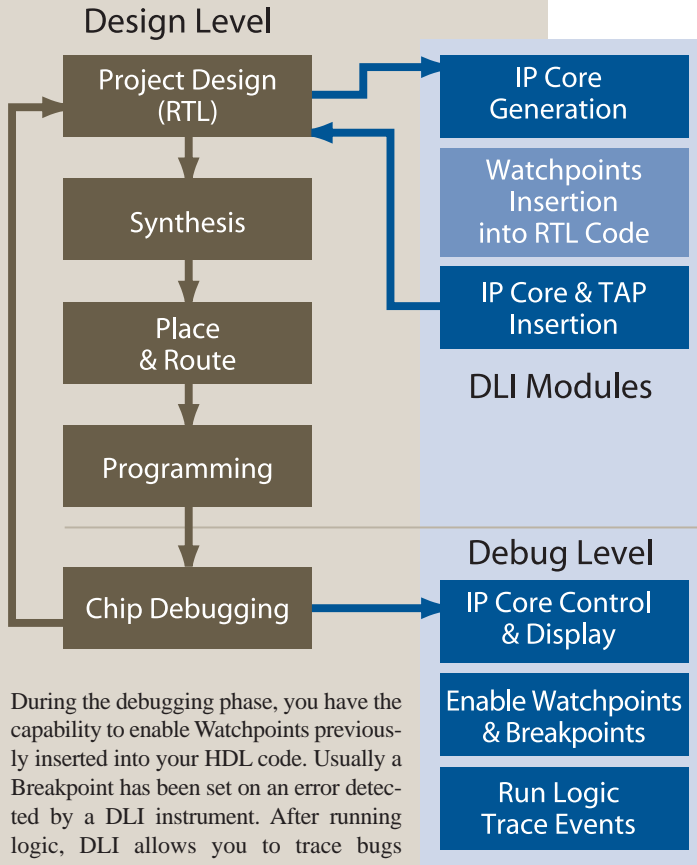
With its powerful and wide range of IP cores, DLI™ increases the verification and debugging capabilities of your system based on high-end FPGA designs or prototypes. IP cores can be combined and associated with multiple trigger conditions to build specific instrumentation and capture data in real-time, at the system clock rate. With an easy connection and simultaneous control of your usual tools, like BDM (Background Debug Mode) and debuggers, a DLI-based debugging strategy can save months of co-debugging effort.

REDUCE YOUR TIME-TO-MARKET

DLI™ offers state-of-the-art embedded testing and provides a clean upgrade path to solve physical access challenges resulting from new packaging technology. Designed to be independent from any PLD Platform, DLI™ tool fits easily into any standard FPGA design flow using a HDL synthesis tool and brings you competitive advantages in terms of debugging cost and time-to-market.



WITH DLI™ INSTRUMENTATION, YOU ARE FREE TO USE ANY FPGA PLATFORM OR SYNTHESIS TOOLS



During the debugging phase, you have the capability to enable Watchpoints previously inserted into your HDL code. Usually a Breakpoint has been set on an error detected by a DLI instrument. After running logic, DLI allows you to trace bugs through events logging and signals recording. The events and user-defined variables analysis is performed conjointly with the code statements leading to fast error-detection of the faulty lines of code.

HDL FF HIGHLIGHTS

- ◆ Automatic & manual Watchpoints insertion
- ◆ Convert any Watchpoint into a Breakpoint during debugging phase
- ◆ Set Breakpoints on instruments or on code
- ◆ Step-by-step code execution, recording & display
- ◆ Concurrent events recording & display
- ◆ Trace & debugging capability up to the instance level
- ◆ Automatic display of trace on Breakpoint
- ◆ Dual display of HDL code versus waveforms

GO QUICKLY STRAIGHT TO THE RTL CODE ERRORS

During the design phase of your hardware, the DLI Core library lets you choose and insert the IP cores instruments needed to perform your debugging process. IP cores are then automatically generated and connected to the internal signals and busses. These cores are inserted into Verilog or VHDL code. At this level, you may insert Watchpoints using the HDL Fault Finder IP, either manually or in automatic mode. Trigger settings and critical user signals to be recorded whenever a Watchpoint is met will also be selected. After synthesis, place and route steps are done using the most current tools available on the market. Finally, the bitstreams are downloaded into the FPGA. DLI Core Control & Display Tool will then enable you to debug your design in real-time; to analyze logic signals levels and transactions, to monitor busses and to record logic events.

HDL Code Window

```

64 if state_register=st5 then
65   if x_int='1' then
66     state_register <- failure;
67     z_int <- '0';
68   else
69     state_register <- success;
70     z_int <- '1';
71   end if;
72 end if;
73 end process;
74
75 z_int <- '1' when state_register=success else '0';
    
```

Wave Viewer

User Defined Variables

Variable	Value
cmd_rec/qa	1:10
cmd_rec/resp	1:10
cmd_rec/qa	1:10
cmd_rec/status	1:10000

Events Logging Window

Automatic Watchpoint Insertion Pop-up

NOW DLI™ AND THE HDL FAULT FINDER GIVE YOU ACCESS TO THE MOST POWERFUL DEBUGGING PLATFORM ON THE MARKET

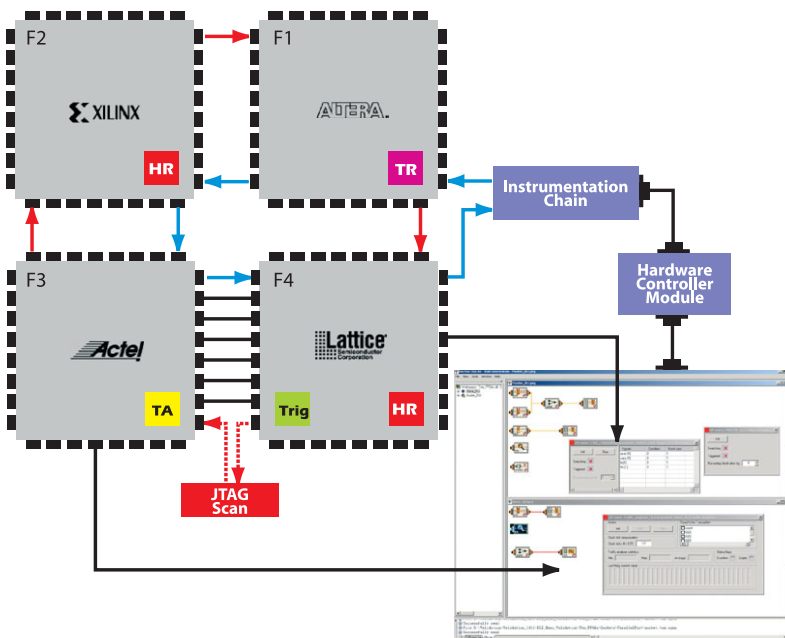


DLI™ MULTI-FPGA POTENTIAL

DiaLite is also able to manage architectures based on multiple FPGA design. DLI provides all you need to instrument your entire system design, before or after the partitioning, whatever the synthesis tool.

Advanced features allow you to instrument either a single FPGA or a complete Multi-FPGA system. This applies even if the system is composed of devices from various manufacturers, as the instrumentation is distributed and controlled through a unique JTAG scan chain.

This gives you a unique capability to do synchronous debugging and make measurements on multiple devices and on multiple clock domains. Trigger signals can be sent from FPGA to FPGA to synchronize instruments located in different devices onto the same clock period. This last feature is particularly valuable in synchronizing BDM or C debuggers with internal transaction recording (real-time trace) and leads to higher efficiency in HW/SW CO-DEBUG.



FEATURES

- ◆ Distributed instrumentation on multiple devices
- ◆ Supports any Actel™, Altera™, Xilinx™, and other FPGA devices or a mix thereof
- ◆ Real synchronization with other tools like BDM and C debugger
- ◆ Dynamically change triggers expected values & LEM equations during debug
- ◆ Supports DCOM scripting interface (C, TCL, Perl)
- ◆ Full independence of System (GCLK) and JTAG (TCK) clocks
- ◆ Step-by-step debugging mode : Instrument results can be read even when GLCK is stopped
- ◆ Fully compatible with major market synthesis tools (Synopsys, Mentor Graphics, Synplicity and others)
- ◆ Large choice of instruments
- ◆ User-definable flow of IP Core instruments
- ◆ Multi-vendor independent platform
- ◆ Multi-languages VHDL (1076.1) and Verilog (1364) design descriptions, or a mix of both
- ◆ Easy tool start-up sequence
- ◆ User Friendly Interface
- ◆ Parallel Port cable, USB or PCI module interface

WHAT'S NEW IN REV 4.6 ?

- ◆ Linux support
- ◆ Partitioning management on Multi-FPGAs platforms
- ◆ State Machine Viewer
- ◆ TemStorage integration, the 1 GB external memory solution for storing large amount of data coming from register-based IPs (HR or TR for example)
- ◆ Support of Xilinx® Native TAP (Spartan™, Virtex™) and Altera® Native TAP (Stratix®, Cyclone™)
- ◆ Mentor Graphics® Precision™ Project Import/Export support in addition to : Quartus® II, Synopsys® DC® FPGA, Synplify Pro®, Libero™, ISE™

DEBUGGING & VERIFICATION TOOLS IN DIALITE™ EDITIONS

DiaLite™ Editions	Assertion Checker	RTL Instrumentation	HOL Fault Finder	Debug Manager
Leading Edge		✓		✓
Power Edge		✓	✓	✓
Platform	✓	✓	✓	✓

DLI™ IP CORES INSTRUMENTATION LIST

<i>IP Family</i>	<i>Name</i>	<i>Use and Benefits</i>
RTL Logic Debug	HDL Fault Finder (FF)	Allows accurate monitoring and display of logic events contained in HDL code that can be traced by inserting Watchpoints and Breakpoints into the source.
RTL Logic Debug	Switches / Leds	Allows the interactive observation of internal signal values and/or to set them to the desired value.
RTL Logic Debug	User Logical Module (ULM)	Allows users to insert or to define their own triggering functions from VHDL or Verilog descriptions. This customized instrumentation can be used either to combine DLI standard triggers, or to detect specific events (State Machine sequences, assertions...)
Logic Analyzer/ Triggers	Glitch Detector (GD)	Allows glitch tracking on sets of signals and generates synchronization for other instruments (internal or external) on the first or more occurrences of the glitch, with a pulse or a flag mode.
Logic Analyzer/ Multi-Conditional Triggers (MCT)	Logic Equation Module (LEM)	Basic qualifier generator, using a real-time adjustable logic equation between a set of two signals or trigger outputs to generate a complex measurement window. Can be chained using multiple LEM and ULM to create a multiple signal logic combination and MCT.
Logic Analyzer/ Triggers	Parallel Trigger (PT)	Allows pattern recognition on a parallel bank of signals. Generates synchronization for other instruments (internal or external) on the first or more occurrences of the expected pattern, with a pulse or flag mode. Also allows precise measurement windows for TA, TR and HR instruments to be defined.
Logic Analyzer/ Triggers	Serial Trigger (ST)	Allows serial pattern recognition on a signal chosen in a bank of signals. Generates synchronization for other instruments (internal or external) on the first or more occurrence of the expected pattern, with a pulse or flag mode. Also allows precise measurement windows for TA, TR and HR instruments to be defined.
Logic Analyzer/ Memory Register	History Register (HR)	Basic recording capability, based on RAM or registers (according to FPGA resources available) allowing a sophisticated logic analyzer to be built with the preceding triggers (in flag mode) and logic equations modules. HR can be associated with Glitch Monitoring capabilities.
Logic Analyzer/ Transaction Register	Transaction Register (TR)	Advanced recording capability based on FPGA RAM blocks allowing the recording of a transaction whatever its duration (Number of clock periods per sample is not a fixed value). Defined by Triggers and Logic Equation Modules, TR can track and capture transactions for long periods of time while saving internal memory resources.
Bus Monitoring	Bus Range Checker (BRC)	Allows capturing any value included within or without a given range of two values or where a value is greater or lesser than a user-defined constant.
Bus Monitoring	Traffic Analyzer (TA)	Analyzes on-chip bus traffic. Monitors DMA cycles (read, write, or all cycles), measures traffic intensity or bus occupancy, tracking any bus faults (stuck, one sense only or saturated). Provides statistics over a long observation period.
Design Robustness	PseudoRandom Generator (PRG)	Allows the generation of pseudo-random patterns on one or more signals to stimulate designs randomly and to check their robustness.

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E-mail : support@temento.com

For more info on Temento Systems solutions, please visit our
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