

DIALITE™ POWER EDGE

PUT PRODUCTIVITY IN YOUR CODE & SIGNAL DEBUGGING

→ BENEFITS

- **The only way to keep observability** into chips while semiconductors trends (Scaling, Integration level, Speed) lead to use packages and design architectures with less or no signals extraction / probing possibilities
- **The widest choice of instruments** (15 instruments among 6 families of IP)
- **A unique productivity and flexibility** when combining the instruments, associating signal instruments and code fault finder or even embedding assertions
- **The true flow independency** as DiaLite exports RTL instrumented designs, while tighter integrations with pre-defined flow (Synthesis, Partitioning) can be achieved with TCL scripts
- **A complete & true collection of solutions for debug & verification:** 3 Editions that take into account the next generation of Debug tools: IP Reuse, System verification, Micro-testers (Protocol checkers, Bus navigators...)
- **The sole technology available on market** to cover all corner cases missed in simulation or emulation
- **Open and gifted for communication** based on standards (VHDL, System Verilog, TCL, C/C++, DCOM)
- **Off-Chip instrumentation:** TemStorage allows to store high amount of test data traces outside the FPGA target
- **Incremental flow* compatibility** allowing to only compile your instrumentation partition
- **Easier to identify the signals that are traced** as DiaLite works at pre-synthesis level with source code reference, while keeping fast debugging

* Date of availability will be announced during 2007

OVERVIEW

DiaLite™ Power Edge provides an unrivaled environment and collection of test IPs to verify and debug your FPGA based system designs:

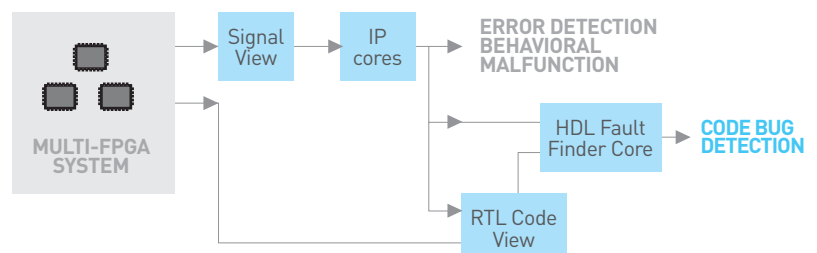
- Trigger on design signal values and sample them at Design Speed
- Run RTL Code Debugger interface to your FPGA Design
- Trace and check AMBA Bus Transaction On-Chip

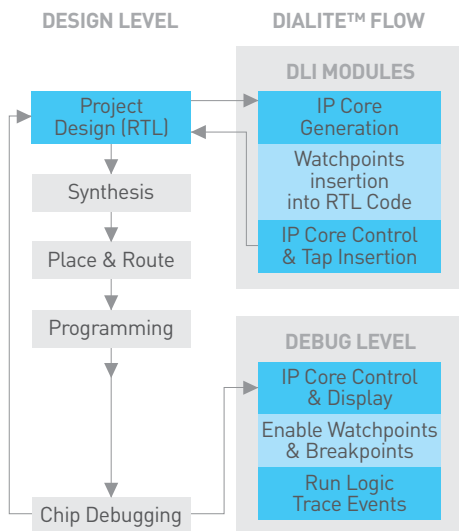
DEBUG YOUR DESIGN CODE ON CHIP AT DESIGN SPEED

With a powerful and wide range of IPs, DiaLite™ increases the verification and debugging capabilities of your design or system environment based on FPGA or prototyping platform. IP cores can be combined and associated with multiple trigger conditions to build specific instrumentation and capture data in real-time. The easy connectivity and extended communication potential of a debugging strategy based on DiaLite™ will save you months of debugging efforts.

A TECHNOLOGY THAT LEADS YOU DIRECTLY TO THE CODE ERROR

The HDL Fault Finder IP allows you to insert WatchPoints and BreakPoints into your HDL code and run concurrently with your signals instrumentation. The HDL Fault Finder provides an accurate monitoring and display of logic events occurring during your debugging session. By simply using a trigger on a signal having suspicious behavior and connecting this trigger as a hardware breakpoint to the HDL Fault Finder, you will be directly pointed to the last lines of code that were executed before the error occurred.





COMPATIBLE WITH ALL FPGA PLATFORMS & SYNTHESIS FLOWS

During the design phase of your hardware, the cores library of DiaLite lets you choose and insert the IP instruments needed to perform your debugging process.

IP cores are then automatically generated and connected to the internal signals and bus. These cores are inserted into Verilog or VHDL code. At this level, Watchpoints can be inserted using the HDL Fault Finder IP, either manually or in automatic mode. Trigger settings and critical user signals to be recorded whenever a Watchpoint is met will also be selected. Synthesis, place and route steps are performed using your usual flow. Finally the bitstream is downloaded into the FPGA whatever your target and manufacturer choice.

Once in debug level, DiaLite enables you to monitor your instrumentation and to debug your design at speed. From a small debugging project to complex system verification, you have all the tools to analyze logic signals, check transactions or protocols, monitor bus and record logic events.

→ HDL FAULT FINDER HIGHLIGHTS & BENEFITS

- Automatic & manual Watchpoint insertion
- Convert any Watchpoint into a Breakpoint during the debugging phase
- Set Breakpoints either on instruments or on your code
- Step-by-step code execution, recording and display
- Concurrent events recording and display
- Trace and debugging capability up to the instance level
- Automatic display of the trace on Breakpoint
- Dual display of HDL code vs. waveforms

CONNECTIVITY THAT BRINGS DEBUG FLEXIBILITY

During your debugging session, you have the opportunity to enable Watchpoints previously inserted into your HDL code. Usually a Breakpoint has been set on error detection with a DiaLite instrument. After running your design up to the fault, DiaLite allows you to trace bugs through events history and signals recording. As the HDL Fault finder is connected and mutually runs with your instrumentation, events and user-defined variables analysis is jointly performed with the code statements. This leads to fast error detection and to directly converge to the faulty lines of code.

- Instrumentation Project
- User Defined Variables
- Events Logging
- Wave viewer
- HDL Code
- State-Machine Viewer
- Watchpoint Manager
- Automatic Watchpoint Insertion
- Traffic Analyzer IP Viewer

A TRUE POTENTIAL FOR YOUR SYSTEM DEBUGGING

DiaLite is well suited to debug a single FPGA design, but can do much more ! The Power Edge Edition has been thought to manage design architectures based on multiple FPGA. Advanced features allow you to instrument a complete multi-FPGAs system, either based on your own board or on a prototyping platform. This applies even if your system is composed of devices from various manufacturers as DiaLite features a unique distributed instrumentation model.

All your instruments are controlled by DiaLite through a single JTAG chain. This gives you a unique capability to perform synchronous debugging and make measurements on multiple devices and on multiple clock domains. Trigger signals can be sent from FPGA to FPGA to synchronize instruments located in different devices on the same clock period.

This last feature is particularly valuable in synchronizing BDM or C debuggers with internal transaction recording and leads to higher efficiency in HW/SW Co-debugging

AMBA BUS ON-CHIP VERIFICATION

It is a fact that most designs implant processor cores and thus embed buses. While many cores and IPs can communicate through these buses, signals tracing can greatly help designers to debug a HW/SW embedded system. DiaLite™ now introduces the first of a new generation of IPs: Bus Trace Analyzer (BTA) and Bus Protocol Checker (BPC*).

AMBA BUS TRACE ANALYZER

This IP is connected to the AMBA system bus and provides signal monitoring and bus tracing. Real-time tracing is achieved with a specific trace compression module, allowing different AMBA bus protocol abstraction level representations. Finally the trace data is stored in a memory on-chip. The tracer can be set up through a JTAG port interface.

AMBA BUS PROTOCOL CHECKER*

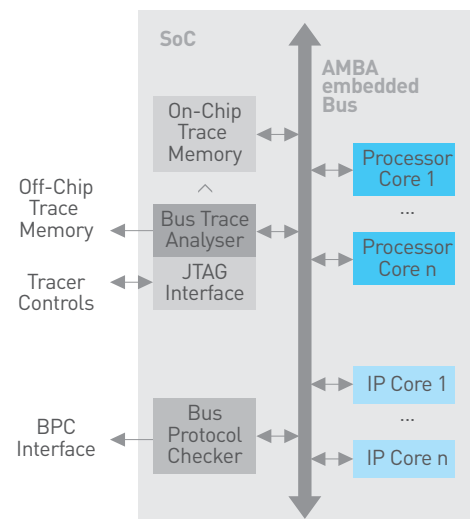
This IP is also connected to the AMBA system bus. It is dedicated to check bus transactions and a is composed of dedicated modules responsible for verifying different rules related to bus entities behaviors (master, slave, decoder, arbiter, signals...). The IP is thus able to check in real-time any default occurring in a bus transaction and to report it for further analysis and debugging.

ALL SEGMENTS, FROM FPGA TO SOC

The DiaLite™ Platform Edition is the most complete environment among all DiaLite™ Editions. Now each DiaLite™ Edition provides the specific debugging and verification tools you need. They range from the basic logical instruments and waveform view to Assertion Checker, HDL Fault Finder and code view. All editions can be extended and complemented according to the verification level you expect and your device target, from small FPGA to SoC.

→ POWER EDGE HIGHLIGHTS

- Incremental flow compatibility for Altera® & Xilinx® targets
- Linux support
- Partitioning management on multi-FPGAs platforms
- State-Machine Viewer
- TemStorage integration: the 1GBytes / 128 channels external memory solution for storing large amount of data coming from register-based IPs like HR
- Support of any FPGA target: Actel®, Altera®, Xilinx®, Lattice® or a combination of them
- Support of Xilinx® Native TAP (Spartan™, Virtex™) and Altera® Native TAP (Stratix®, Cyclone™, ProAsic 3, ProAsic 3E, 500K, Fusion)
- Project Import/Export support to: Mentor Graphics® Precision™, Quartus® II, Synplify Pro®, Libero™, ISE™



→ DIALITE™ EDITIONS

	Leading Edge	Power Edge	Platform
RTL INSTRUMENTATION	•	•	•
DEBUG MANAGER	•	•	•
HDL FAULT FINDER	-	•	•
PSL / SVA ASSERTION CHECKER	-	-	•
AMBA BPA / BPC	op.	op.	op.

“•”: included, “-”: non included, “op.”: optional

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DIALITE™ POWER EDGE

→ DIALITE™ IP CORES INSTRUMENTATION LIST

IP FAMILY	IP NAME	USE AND BENEFITS
RTL Logic Debug	HDL Fault Finder (FF)	Allows accurate monitoring and display of logic events contained in your HDL code that can be traced by inserting Watchpoints and Breakpoints into the source (Option).
RTL Logic Debug	Switches / Leds	Allows interactively observing internal signal values and/or driving them to the desired value.
RTL Logic Debug	User Logical Module (ULM)	Allows users to insert or to define their own triggering functions from VHDL or Verilog descriptions. This customized instrumentation can be used either to combine DiaLite™ standard triggers or to detect specific events (State Machine sequences, assertions...).
Logic Analyzer/ Trigger	Glitch Detector (GD)	Allows glitch tracking on sets of signals and generates synchronization for other instruments (internal or external) on the first or more occurrence of a glitch, using pulse or flag mode.
Logic Analyzer/ Multi Conditional Trigger (MCT)	Logic Equation Module (LEM)	Basic qualifier generator, using a real-time adjustable logic equation between a set of two signals or trigger outputs to generate a complex measurement window. Can be chained using multiple LEM and ULM to create a multiple signal logic combination and MCT.
Logic Analyzer/ Trigger	Parallel Trigger (PT)	Allows pattern recognition on a parallel bank of signals and generates synchronization for other instruments (internal or external) on the first or more occurrence of the expected pattern, using pulse or flag mode.
Logic Analyzer/ Trigger	Serial Trigger (ST)	Allows the serial pattern recognition on a signal chosen from a bank of signals and generates synchronization for other instruments (internal or external) on the first or more occurrence of the expected pattern, using pulse or flag mode.
Logic Analyzer/ Memory Register	History Register (HR)	Basic recording capability, based on RAM or registers (according to FPGA resources available) allows building a sophisticated logic analyzer with preceding triggers (in flag mode) and logic equations modules. HR can be associated with Glitch Monitoring capabilities.
Logic Analyzer/ Transaction Register	Transaction Register (TR)	Advanced recording capability based on FPGA RAM blocks allowing the recording of a transaction whatever its duration. Defined by Triggers and Logic Equation Modules, TR can track and capture transactions for long periods of time while saving internal memory resources.
Counter	Counter (CTR)	Allows to trigger on an event after a fixed duration or after a fixed occurrence of an event. It is also possible to trigger if a signal pulse is too short.
Bus Monitoring	Bus Range Checker (BRC)	Allows capturing any value included inside or outside a given range defined by two values or a value higher or lower than a user-defined constant.
Bus Monitoring	Bus Trace Analyzer (BTA)	Allows monitoring and dumping bus trace after resolution encoding and data compression computing. Data trace is stored On or Off Chip for further analysis.
Bus Monitoring	Bus Protocol Checker (BPC)*	Allows checking bus transactions according to a set of defined rules related to bus entities behaviors (master, slave, arbiter...).
Bus Monitoring	Traffic Analyzer (TA)	Analyzes bus traffic on-chip. Monitors DMA cycles (read, write, or all cycles), measures traffic intensity or bus occupancy. Tracks any faulty bus (stuck, one sense only or saturated). Provides statistics over a long observation period.
Design Robustness	PseudoRandom Generator (PRG)	Allows the generation of pseudo random patterns on one or more signals to stimulate designs randomly and to check their robustness.

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www.temento.com

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